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1 Dedicated circuits: A programmable cellular neural network circuit

Michel Leong, Pedro Vasconcelos, Jorge R. Fernandes, Leonel Sousa

September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**

Full text available: pdf(695.99 KB) Additional Information: full citation, abstract, references, index terms

In this paper we propose and develop a fully programmable CNN circuit. The CNN coefficients are digitally programmable using a Digital to Analog Converter (DAC), resulting in added flexibility.CNNs with 4x4 and 16x16 cells are designed and tested, exhibiting good accuracy when compared with Matlab and Java applications for computing CNNs.All circuits are designed and implemented with a 0.35um CMOS technology. The layout of a full 4x4 CNN was designed using Cadence Design Framework II. The circui ...

Keywords: VLSI, cellular neural networks, microelectronics

2 A BIST scheme for on-chip ADC and DAC testing

Jiun-Lang Huang, Chee-Kian Ong, Kwang-Ting Cheng

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(114.67 KB) Publisher Site Additional Information: full citation, references, citings, index terms

3 Power grid design and analysis techniques: Efficient power/ground network analysis for power integrity-driven design methodology

Su-Wei Wu, Yao-Wen Chang

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(177.31 KB) Additional Information: full citation, abstract, references, index terms

As technology advances, the metal width is decreasing with the length increasing, making the resistance along the power line increase substantially. Together with the nonlinear scaling of the threshold voltage that makes the ratio of the threshold voltage to the supply voltage rise, the voltage (IR) drop become a serious problem in modern VLSI design. Traditional power/ground (P/G) network analysis methods are typically very computationally expensive and thus not feasible to be integrated into f ...

Keywords: footnotesize floorplanning, power/ground network

4 Current signature compression for IR-drop analysis
Rajat Chaudhry, David Blaauw, Rajendran Panda, Tim Edwards
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(384.04 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a novel approach to compress current signatures for IR-drop analysis of large power grids. Our approach divides the original current signature into error bounded compression sets. Each compression set has a representative timepoint. The compressed current signature consists of the representative timepoints. The compression technique exploits the pattern of change of individual currents, time locality and periodicity to achieve very high quality results. We provide error g ...

5 Future performance challenges in nanometer design
Dennis Sylvester, Himanshu Kaul
June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(252.60 KB) Additional Information: full citation, abstract, references, citings, index terms

We highlight several fundamental challenges to designing high-performance integrated circuits in nanometer-scale technologies (i.e. draRita Glover, EDA Today, L.C.wn feature sizes< 100 nm). Dynamic power scaling trends lead to major packaging problems. To alleviate these concerns, tMarc Halpernhermal monitoring and feedback mechanisms can limit worst-case dissipation and reduce costs. Furthermore, a flexible multi-Vdd + multi-Vth + re-sizing approach is advocated to leverage the inherent pr ...

6 Energy and thermal-aware design: Theoretical and practical limits of dynamic voltage scaling
Bo Zhai, David Blaauw, Dennis Sylvester, Krisztian Flautner
June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(222.66 KB) Additional Information: full citation, abstract, references, index terms

Dynamic voltage scaling (DVS) is a popular approach for energy reduction of integrated circuits. Current processors that use DVS typically have an operating voltage range from full to half of the maximum Vdd. However, it is possible to construct designs that operate over a much larger voltage range: from full Vdd to subthreshold voltages. This possibility raises the question of whether a larger voltage range improves the energy efficiency of DVS. First, from a theoretical point of view, we show ...

Keywords: dynamic voltage scaling, minimum energy point

7 12-b 125 MSPS CMOS D/A designed for spectral performance
D. Mercer, L. Singer
August 1996 **Proceedings of the 1996 international symposium on Low power electronics and design**

Full text available: pdf(223.48 KB) Additional Information: full citation, references, index terms

8 Power grid design and analysis techniques: A stochastic approach To power grid analysis
Sanjay Pant, David Blaauw, Vladimir Zolotov, Savithri Sundareswaran, Rajendran Panda
June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(312.28 KB) Additional Information: full citation, abstract, references, index terms

Power supply integrity analysis is critical in modern high perfor-mance designs. In this paper, we propose a stochastic approach to obtain statistical information about the collective IR and LdI/dt drop in a power supply network. The currents drawn from the power grid by the blocks in a design are modelled as stochastic processes and their statistical information is extracted, including correlation infor-mation between blocks in both space and time. We then propose a method to propagate the stat ...

Keywords: IR drop, Ldi/dt, power supply networks

9 SOI Transistor Model for Fast Transient Simulation

D. Nadezhin, S. Gavrilov, A. Glebov, Y. Egorov, V. Zolotov, D. Blaauw, R. Panda, M. Becer, A. Ardelea, A. Patel

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(164.09 KB) Additional Information: full citation, abstract, index terms

Progress in semiconductor process technology has made SOItransistors one of the most promising candidates for high performanceand low power designs. With smaller diffusion capacitances,SOI transistors switch significantly faster than theirtraditional bulk MOS counterparts and consume less power perswitching. However, design and simulation of SOI MOS circuits ismore challenging due to more complex behavior of an SOI transistorinvolving floating body effects, delay dependence on history oftransist ...

10 Session 6D: Analog synthesis: The sizing rules method for analog integrated circuit design

H. Graeb, S. Zizala, J. Eckmueller, K. Antreich

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(221.02 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents the *sizing rules method* for analog CMOS circuit design that consists of: first, the development of a hierarchical library of transistor pair groups as basic building blocks for analog CMOS circuits; second, the derivation of a hierarchical generic list of constraints that must be satisfied to guarantee the function of each block and its reliability with respect to physical effects; and third, the development of an automatic recognition of building blocks in a circuit s ...

11 Efficient and accurate testing of analog-to-digital converters using oscillation-test method

K. Arabi, B. Kaminska

March 1997 **Proceedings of the 1997 European conference on Design and Test**

Full text available: pdf(511.01 KB) Publisher Site Additional Information: full citation, abstract

This paper describes a practical test approach for analog-to-digital converters (ADCs) based on the oscillation-test strategy. The oscillation-test is applied to convert the ADC under test to an oscillator. The oscillation frequencies are able to monitor the ADC conversion rate, differential nonlinearity (DNL) and integral nonlinearity (INL) at each quantization band edge (QBE). Using this method, no analog stimulus should be supplied and therefore the need for a costly precision signal generato ...

Keywords: A/D convertor, ADC conversion rate, ADC testing, analog-to-digital converters, analogue-digital conversion, differential nonlinearity, digital circuitry, integral nonlinearity, oscillation-test method, quantization band edge

12 Hierarchical analysis of power distribution networks

Min Zhao, Rajendran V. Panda, Sachin S. Sapatnekar, Tim Edwards, Rajat Chaudhry, David Blaauw

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(206.93 KB) Additional Information: full citation, abstract, references, citings, index terms

Careful design and verification of the power distribution network of a chip are of critical importance to ensure its reliable performance. With the increasing number of transistors on a chip, the size of the power network has grown so large as to make the verification task very challenging. The available computational power and memory resources impose limitations on the size of networks that can be analyzed using currently known techniques. Many of today's designs have power network ...

13 Preservation of passivity during RLC network reduction via split congruence transformations

Kevin J. Kerns, Andrew T. Yang

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: pdf(68.70 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

None of the existing network reduction tools preserve passivityfor RLC networks. The loss of passivity can be a serious problembecause simulations of the reduced networks may encounter"time step too small" errors. This paper presents a set oftransformations called "Split Congruence Transformations"(SCT's) which can be used to accurately reduce a RLC networkwhile preserving passivity.

14 Reliability-constrained area optimization of VLSI power/ground networks via sequence of linear programmings

Xiang-Dong Tan, C.-J. Richard Shi, Dragos Lungeanu, Jyh-Chwen Lee, Li-Pen Yuan

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(94.52 KB) Additional Information: full citation, references, citings, index terms

15 A capacitor-based D/A converter with continuous time output for low-power applications

Lapoe Lynn, Paul Ferguson

August 1997 **Proceedings of the 1997 international symposium on Low power electronics and design**

Full text available: pdf(533.42 KB) Additional Information: full citation

16 A 16 Bit + Sign Monotonic Precise Current DAC for Sensor Applications

Pavel Horský

February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 3**

Full text available: Publisher Site Additional Information: full citation, abstract

A 16 bit + sign monotonic precise current DAC for sensor applications working in a harsh environment is described. It is working in a wide temperature range with high output voltage swing and low current consumption.The converter is based on current division and segmentation techniques to guarantee monotonicity. Two active cascoding loops and one follower loop are used to improve the output impedance, the accuracy and the voltage compliance of the DAC. The resolution of the DAC is further increa ...

17 Design space exploration and scheduling for embedded software: Leakage aware dynamic voltage scaling for real-time embedded systems
Ravindra Jejurikar, Cristiano Pereira, Rajesh Gupta
June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(109.61 KB) Additional Information: full citation, abstract, references, citings, index terms

A five-fold increase in leakage current is predicted with each technology generation. While Dynamic Voltage Scaling (DVS) is known to reduce dynamic power consumption, it also causes increased leakage energy drain by lengthening the interval over which a computation is carried out. Therefore, for minimization of the total energy, one needs to determine an operating point, called the *critical speed*. We compute processor slowdown factors based on the critical speed for energy minimization. ...

Keywords: EDF scheduling, critical speed, leakage power, low power scheduling, procrastication, real-time systems

18 Novel design methodologies and signal integrity: Statistical estimation of leakage-induced power grid voltage drop considering within-die process variations
Imad A. Ferzli, Farid N. Najm
June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(257.93 KB) Additional Information: full citation, abstract, references, index terms

Transistor threshold voltages *Vth* have been reduced as part of on-going technology scaling. The smaller Vth values feature increased fluctuations due to process variations, with a strong within-die component. Correspondingly, given the exponential dependence of leakage on.*Vth*, circuit leakage currents are increasing significantly and have strong within-die statistical variations. With these currents loading the power grid, the grid develops large voltage drops, which is an unavoida ...

Keywords: leakage current, power grid, statistical analysis, voltage drop

19 Maximum voltage variation in the power distribution network of VLSI circuits with RLC models
Sudhakar Bobba, Ibrahim Hajj
August 2001 **Proceedings of the 2001 international symposium on Low power electronics and design**

Full text available: pdf(245.18 KB) Additional Information: full citation, references, citings, index terms

20 A mixed nodal-mesh formulation for efficient extraction and passive reduced-order modeling of 3D interconnects
Nuno Marques, Mattan Kamon, Jacob White, L. Miguel Silveira
May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(363.76 KB) Additional Information: full citation, abstract, references, citings, index terms

Publisher Site

As VLSI circuit speeds have increased, reliable chip and system design can no longer be performed without accurate three-dimensional interconnect models. In this paper, we describe an integral equation aproach to modeling the impedance of inter-connect structures accounting for both the charge accumulation on the surface of conductors and the current traveling in their interior: Our formulation, based on a combination of nodal and mesh analysis, has the required properties to be combined wi ...

Keywords: congestion, global routing, quadratic placement, relaxed pins, routing models, supply-demand

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